Listing of the Claims

1. (original) A method for an improved polysilicon etching process for forming self-aligned polysilicon micro-integrated circuit structures without protruding polysilicon portions comprising the steps of:

providing a semiconductor wafer process surface comprising first exposed polysilicon portions and adjacent oxide portions;

forming a first oxide layer on the exposed polysilicon portions;

blanket depositing a polysilicon layer on the first exposed polysilicon portions and adjacent oxide portions;

forming a hard mask layer on the polysilicon layer;

carrying out a multi-step reactive ion etching (RIE) process to etch through the hardmask layer and etch through a thickness portion of the polysilicon layer to form second polysilicon portions adjacent the oxide portions having upward protruding outer polysilicon fence portions;

contacting the semiconductor wafer process surface with an aqueous HF solution; and,

carrying out a downstream plasma etching process to remove polysilicon fence portions.

2. (original) The method of claim 1, wherein the multi-step RIE etching step further comprises:

etching through a thickness of the hardmask layer in a first etching step;

etching through a thickness portion of the polysilicon layer to form the second polysilicon portions in a second etching step;

blanket forming a second oxide layer over second polysilicon portions;

etching through a thickness portion of the second oxide layer to expose the second polysilicon silicon portions and first oxide layer in a third etching step; and,

over-etching the second polysilicon portions to endpoint in a fourth etching step.

3. (original) The method of claim 2 wherein the second etching step comprises an etching chemistry including $CF_4/HBr/Cl_2/He\text{-}O_2$.

4. (original) The method of claim 2 wherein the overetching step comprises a chlorine-free etching chemistry.

5. (original) The method of claim 4 wherein the chlorine free etching chemistry comprises $HBr/He\text{-}O_2$.

6. (original) The method of claim 1, wherein the step of forming the first oxide layer is a thermal growth process.

7. (original) The method of claim 2, wherein the step of forming the second oxide layer comprises an in situ oxygen plasma process.

8. (original) The method of claim 1, wherein the step of contacting the semiconductor wafer process surface with an aqueous HF solution comprises a dipping process.

9. (original) The method of claim 1, wherein the aqueous HF solution comprises an HF concentration of 0.3 to 0.7 volume percent HF in deionized water with respect to a solution volume.

10. (original) The method of claim 1, wherein the downstream plasma etching process comprises a chemical dry etching (CDE) process including etching chemistry including CF_4 and O_2.

11. (original) The method of claim 1, further comprising the step of contacting the semiconductor wafer process surface with an aqueous HF solution following the step of carrying out a downstream plasma etching process.

12. (original) A method for an improved polysilicon etching process for forming square shouldered self-aligned polysilicon word line electrodes in a split-gate FET configuration comprising the steps of:

providing a semiconductor wafer process surface comprising a polysilicon source electrode including adjacent polysilicon floating gate electrodes and oxide spacers overlying the polysilicon floating gate electrodes;

thermally growing a first oxide layer on exposed polysilicon portions;

blanket depositing a polysilicon layer on the semiconductor wafer process surface;

forming a silicon oxide hardmask layer on the polysilicon layer;

reactive ion etching (RIE) through the hardmask layer thickness in a first etching step;

reactive ion etching (RIE) through a thickness portion of the polysilicon layer to partially form polysilicon wordline portions adjacent the oxide spacers in a second etching step;

plasma forming a second oxide layer over second polysilicon portions according to an oxygen plasma process;

reactive ion etching (RIE) through a thickness portion of the second oxide layer to expose the second polysilicon silicon portions and first oxide layer in a third etching step;

reactive ion etching (RIE) the second polysilicon portions to endpoint in a fourth etching step including forming upward protruding polysilicon fences at an outer portion of the second polysilicon portions;

contacting the semiconductor wafer process surface with an aqueous HF solution; and,

carrying out a downstream plasma etching process comprising a CF_4 and O_2 etching chemistry to remove the polysilicon fences.

13. (original) The method of claim 12, wherein the second etching step comprises an etching chemistry including $CF_4/HBr/Cl_2/He-O_2$.

14. (original) The method of claim 12, wherein the fourth etching step comprises a chlorine-free etching chemistry.

15. (original) The method of claim 12 wherein the chlorine free etching chemistry comprises $HBr/He-O_2$.

16. (original) The method of claim 12, wherein the step of contacting the semiconductor wafer process surface with an aqueous HF solution comprises a dipping process.

17. (original) The method of claim 12, wherein the aqueous HF solution comprises an HF concentration of 0.3 to 0.7 volume percent HF in deionized water with respect to a solution volume.

18. (original) The method of claim 12, wherein the downstream plasma etching process comprises a chemical dry etching (CDE) process including etching chemistry including CF_4 and O_2.

19. (original) The method of claim 12, further comprising the step of contacting the semiconductor wafer process surface with an aqueous HF solution following the step of carrying out a downstream plasma etching process.

20. (original) The method of claim 12, wherein the second etching step comprises fluorocarbon/O_2 etching chemistry.

21. - 26. (Cancelled)